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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,857	03/31/2004	Robert E. Cypher	5681-13501	5571

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EXAMINER	
ELAND, SHAWN	
ART UNIT	**PAPER NUMBER**
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,857	CYPHER, ROBERT E.	
	Examiner	Art Unit	
	Shawn Eland	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004 02 Sept. 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/11/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 48 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Liencres et al.*** (US 5,434,993).

In regards to claim 1, Liencres teaches a plurality of nodes ***(see element 20 in figure 3a; see column 6, lines 13 – 15)*** coupled by an inter-node network ***(see element 31)***, wherein each node includes a plurality of active devices ***(see elements 21 & 35)***, a memory subsystem ***(see element 32)***, and an address network and a data network respectively configured to convey address packets and data packets between the plurality of active devices and the memory subsystem ***(see element 31)***; wherein a memory subsystem included in a node of the plurality of nodes is configured to maintain a response indication indicating whether the memory subsystem should send a data packet corresponding to a coherency unit in response to receiving from an active device in the node an address packet requesting an access right to the coherency unit ***(see column 7, "Read Transactions")***; wherein the node is configured to store a node identifier for the coherency unit, wherein the node identifier identifies a different node of the plurality nodes in which the coherency unit is in a modified global access state ***(see column 7, lines 7 – 10)***.

In regards to claim 17, Liencres teaches a plurality of client devices ***(see element 20 in figure 3a; see column 6, lines 13 – 15)*** including a memory subsystem ***(see element 32)***, an active device ***(see element 21)***, and an interface configured to send and receive coherency messages on an inter-node network coupling nodes in the multi-node computer system ***(see element 31)***; an address network configured to convey address packets between the plurality of client devices ***(see element 33)***; a data network configured to convey data packets between the plurality of client devices ***(see element 33)***; wherein the memory is configured to maintain a response indication indicating whether the memory should send a data packet corresponding to a coherency unit on the data network in response to receiving an address packet requesting an access right to the coherency unit from the active device ***(see column 7, "Read Transactions")***; wherein the node is configured to store a node identifier for the coherency unit, wherein the node identifier identifies a different node in the multi-node system in which the coherency unit is in a modified global access state ***(see column 7, lines 7 – 10)***.

In regards to claim 33, Liencres teaches wherein the multi-node computer system includes a plurality of nodes coupled by an inter-node network ***(see elements 20 & 25 in figure 3a)***, wherein each node includes an active device ***(see element 21)***, a memory subsystem ***(see element 32)***, and an address network coupling the active device and the memory subsystem ***(see element 33)***, the method comprising: a memory subsystem included in a node of the plurality of nodes receiving from an active device included in the node an address packet requesting an access right to a

coherency unit ***(see column 7, "Read Transactions")***; in response to said receiving, the memory subsystem sending a responsive data packet to the active device dependent on response indication associated with the coherency unit ***(see column 7, "Read Transactions")***; the node sending a coherency message requesting the access right to a different node of the plurality of nodes in response to a node identifier identifying the different node as a node in which the coherency unit is in a modified global access state ***(see column 7, "Read Transactions")***.

In regards to claim 2, Liencres teaches wherein each node includes an interface coupled to send and receive coherency messages on the inter-node network ***(see element 31)***, wherein an interface included in the node is configured to store the node identifier for the coherency unit ***(see column 7, lines 7 – 19)***.

In regards to claim 18, Liencres teaches wherein the interface is configured to store the node identifier for the coherency unit ***(see column 7, lines 7 – 10)***.

In regards to claim 34, Liencres teaches storing the node identifier for the coherency unit and sending the coherency message to the different node ***(see column 7, lines 7 – 19)***.

In regards to claims 3 & 19, Liencres teaches wherein the interface is configured to store the node identifier in a global information cache that includes storage for a plurality of node identifiers for a plurality of coherency units ***(see element 46)***.

In regards to claim 35, Liencres teaches wherein said storing comprises the interface storing the node identifier in a global information cache that includes storage for a plurality of node identifiers for a plurality of coherency units ***(see element 46)***.

In regards to claims 4 & 20, Liencres teaches wherein the interface included in the node is further configured to store a global access state of the coherency unit in the node ***(see column 7, lines 7 – 10; see column 1, lines 64 – 65)***.

In regards to claim 36, Liencres teaches the interface storing a global access state of the coherency unit in the node ***(see column 7, lines 7 – 10; see column 1, lines 64 – 65)***.

In regards to claims 5 & 21, Liencres teaches wherein in response to receiving a coherency message sent by another one of the nodes requesting an access right to the coherency unit, the interface is configured to access the node identifier and to responsively send an additional coherency message to an interface included in the different node ***(see column 7, "Read Transactions")***.

In regards to claim 37, Liencres teaches in response to receiving a coherency message sent by another one of the nodes requesting an access right to the coherency unit, the interface sending an additional coherency message to an interface included in the different node identified by the node identifier ***(see column 7, "Read Transactions")***.

In regards to claim 6, Liencres teaches wherein in response to receiving yet another coherency message acknowledging that the other one of the plurality of nodes gained the access right to the coherency unit, the interface included in the node is configured to update the node identifier to identify the other one of the plurality of nodes if an active device included in the other one of the plurality of nodes gained write access to the coherency unit ***(see column 7, "Write Transactions")***.

In regards to claim 22, Liencres teaches wherein in response to receiving yet another coherency message acknowledging that the other one of the plurality of nodes gained the access right to the coherency unit, the interface is configured to update the node identifier to identify the other one of the plurality of nodes if an active device included in the other one of the plurality of nodes gained write access to the coherency unit ***(see column 7, "Write Transactions")***.

In regards to claim 38, Liencres teaches in response to receiving yet another coherency message acknowledging that the other one of the plurality of nodes gained the access right to the coherency unit, the interface updating the node identifier to identify the other one of the plurality of nodes if an active device included in the other one of the plurality of nodes gained write access to the coherency unit ***(see column 7, "Write Transactions")***.

In regards to claim 7, Liencres teaches wherein if the interface included in the node updates the node identifier, the interface is configured to send an address packet indicating a new value of the node identifier to the memory subsystem included in the node ***(see column 7, "Write Transactions"; see elements 34 & 46; see column 6, lines 64 – 67; see column 7, lines 7 – 10)***.

In regards to claim 23, Liencres teaches wherein if the interface updates the node identifier, the interface is configured to send an address packet indicating a new value of the node identifier to the memory subsystem ***(see column 7, "Write Transactions"; see elements 34 & 46; see column 6, lines 64 – 67; see column 7, lines 7 – 10)***.

In regards to claim 39, Liencres teaches the interface sending an address packet indicating a new value of the node identifier to the memory subsystem if the interface updates the node identifier ***(see column 7, "Write Transactions"; see elements 34 & 46; see column 6, lines 64 – 67; see column 7, lines 7 – 10)***.

In regards to claims 8 & 24, Liencres teaches wherein the memory subsystem is configured to update the response indication in response to receiving address packets from one or more active devices included in the node ***(see column 8, lines 13 – 32)***.

In regards to claim 40, Liencres teaches the memory subsystem updating the response indication in response to receiving address packets from one or more active devices included in the node ***(see column 8, lines 13 – 32; the data is prepared for write-back)***.

In regards to claims 9, 25, & 41, Liencres teaches updating the response indication to indicate that the memory subsystem should not respond to address packets requesting an access right to the coherency unit in response to receiving an address packet requesting a write access right to the coherency unit from one of the one or more active devices ***(see column 8, lines 33 – 46)***.

In regards to claims 10, 26, & 42, Liencres teaches updating the response indication to indicate that the memory subsystem should respond to address packets requesting an access right to the coherency unit in response to receiving an address packet requesting to write a new value of the coherency unit to the memory subsystem ***(see column 8, lines 63 – 68; write-back should stop)***.

In regards to claims 11, 27, & 43, Liencres teaches not updating the response indication in response to address packets requesting a shared access right to the coherency unit ***(see column 9, lines 1 – 8)***.

In regards to claims 12, 28, & 44, Liencres teaches the memory subsystem sending a packet corresponding to the address packet to the interface if: the response indication indicates that the memory should not respond; the coherency unit is in a shared global access state in the node; and the address packet requests write access to the coherency unit ***(see column 8, lines 33 – 46)***.

In regards to claims 13 & 29, Liencres teaches wherein in response to the packet corresponding to the address packet, the interface is configured to send a coherency message requesting write access to the coherency unit to the different node identified by the node identifier ***(see column 7, "Write Transactions")***.

In regards to claim 45, Liencres teaches the interface sending a coherency message requesting write access to the coherency unit to the different node identified by the node identifier in response to receiving the packet corresponding to the address packet ***(see column 7, "Write Transactions")***.

In regards to claims 14, 30, & 46, Liencres teaches sending a packet corresponding to the address packet to the interface if: the response indication indicates that the memory should not respond; and the coherency unit is in an invalid global access state in the node ***(see column 8, lines 63 – 68)***.

In regards to claim 15, Liencres teaches the node is configured to update the node identifier in response to receiving coherency messages from other ones of the plurality of nodes via the inter-node network ***(see column 7, "Write Transactions")***.

In regards to claims 31 & 47, Liencres teaches the node updating the node identifier in response to the interface receiving coherency messages from other nodes in the multi-node system ***(see column 7, "Write Transactions")***.

In regards to claims 16, 32, & 48, Liencres teaches an active device that sends the address packet specifying the coherency unit gaining the access right to the coherency unit in response to receiving the data packet from the memory subsystem if the memory subsystem sends the data packet ***(see column 7, "Write Transactions")***.

Examiner Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Eland whose telephone number is (571) 270-1029. The examiner can normally be reached on Tuesday – Thursday from 7:30am to 5:00pm. The examiner can also be reached on alternate Mondays & Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough, can be reached on (571) 272-4199. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn Eland
01/04/2007

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
1-5-06